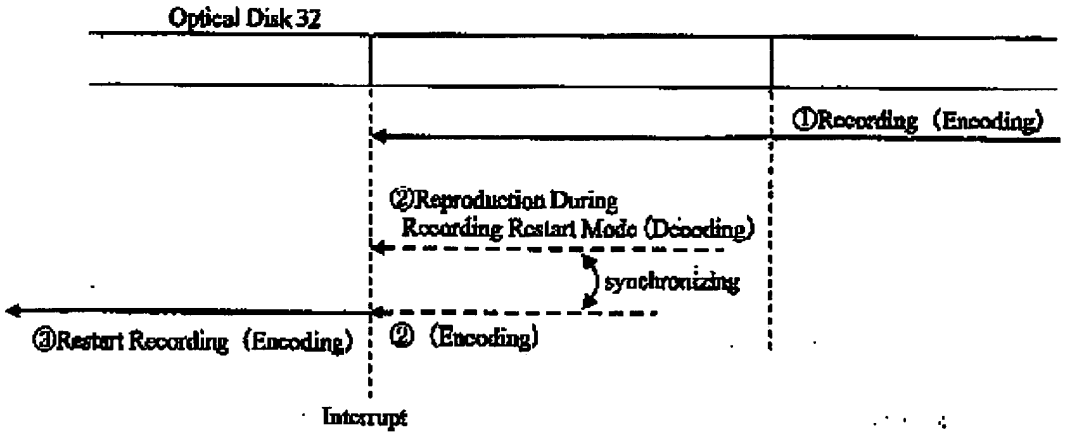
2) a first retry determination circuit for determining whether an address of written data, which is read from a recording medium, and an address of read data, which is provided to an encoder from a buffer memory, are the same, 3) a second retry determination circuit for determining whether a timing for reading the written data from the recording medium and a timing for encoding the read data are the same, and 4) a restart circuit for restarting the writing of data to the recording medium based on the determinations of the first and second retry determination circuits.

The present invention relates to techniques for writing new data to correctly and continuously connect the new data with data recorded on a recording medium. In one particular example, as shown in Fig. 2, when a data recording operation for recoding data on an optical disk 32 is interrupted in a first step, a second step of data reproduction in a recording restart mode is started. In the second step, a decoder generates decoded data written on the recording medium, and an encoder generates encoded data substantially corresponding to the position where the encoded data is written. Then, the decoded data and the encoded data are synchronized each other. The first and second retry determination circuits determined whether it is possible to shift a third step for continuously writing data subsequent to the data recorded at the interrupted position in the first step.

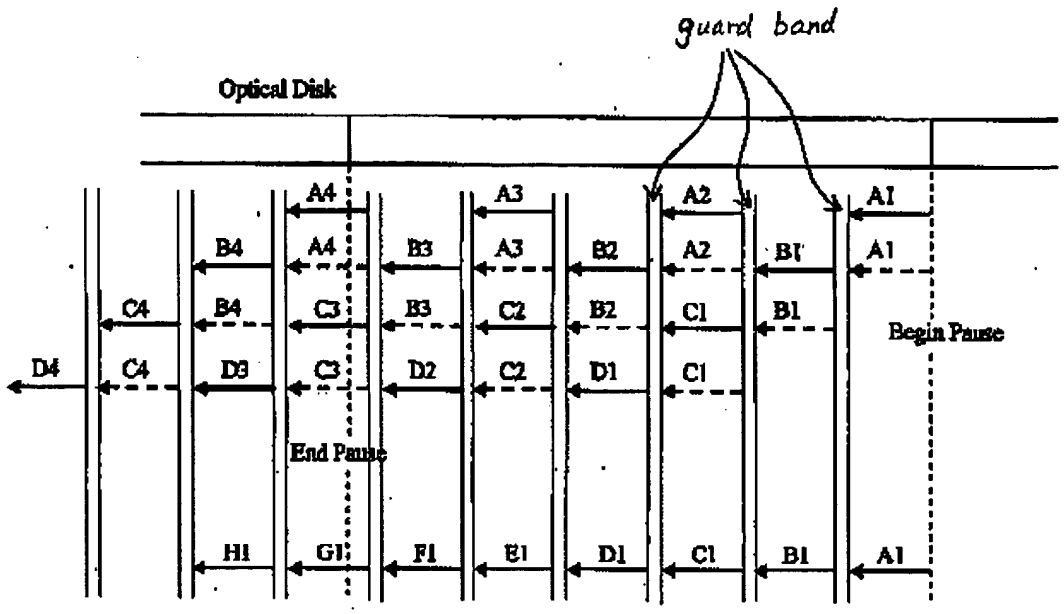


Willis discloses data buffer management and a method for assigning record segments and play back recorded segments on a disk after a pause. Willis records data onto alternate segments

of a track when a pause operation is started and initiates complementary operation of record and track buffers when a recording operation is restarted from the pause starting position.

Specifically, when a pause operation is started, data is recorded on an optical disk in a predetermined interval. This recording continues to a last segment subsequent to the pause end position. When a recording operation is restarted, a reproducing operation and a writing operation are repeated. The reproducing operation reproduces data recorded during the pause operation and the writing operation writes data at the portions where data is not recorded on the optical disk, thereby simultaneously performing current data writing and past data reproducing.

More specifically, as shown in the following figure, plural pieces of data A1-A4 are recorded in a predetermined interval during a pause operation. When a recording operation is restarted, data A1 reproduction and data B1 recording, data A2 reproduction and data B2 recording, data A3 reproduction and data B3 recording, and data A4 reproduction and data B4 recording are sequentially performed. Then, data B1 reproduction and data C1 recording, data B2 reproduction and data C2 recording, data B3 reproduction and data C3 recording, and data B4 reproduction and data C4 recording are sequentially performed. The operation like above is performed repeatedly. At this time, pieces of data A1, B1, C1, D1, E1 ... are finally recorded on an optical disk. In other words, pieces of data A2-A4, B2-B4, C2-C4, D2-D4, and E2-E4 do not remain as records. Guard bands 22 are respectively provided at regions each defined between adjacent segments in order to prevent over writing when a recording operation is not quickly performed between reproduction and recording.



The following is a comparison between the present invention recited in claim 1 and Willis.

(1) Synchronizing circuit

The Examiner states that Willis discloses the synchronizing circuit at column 8, lines 37-49 and column 8, lines 61-67. However, Willis does not disclose such a synchronizing circuit. The synchronizing circuit of the present invention synchronizes written data read from a recording medium with encoded data read from a buffer.

In contrast, Willis describes a technique concerning a bit rate of an encoder and a decoder and does not describe a technique concerning synchronization through the specification. Since there is no continuity between reproducing data (e.g. A1) and recording data (e.g. B1), it is not necessary to synchronize the reproducing data (written data) and the recording data (encoded data). Accordingly, Willis does not disclose the synchronizing circuit of the present invention.

(2) First entry determination circuit

The Examiner states that Willis discloses the first entry determination circuit because matching address as of a write data and a read data is a process of recording the data into a

proper track address which is provided by the encoding means at Figs. 1 and 3. The first entry determination circuit of the present invention determines whether an address of write data, which is read from a recording medium, and an address of read data, which is provided to an encoder from a buffer memory, is the same. When data synchronization is taken by the synchronizing circuit, these addresses are the same.

In contrast, although Willis describes track addresses at Figs. 1 and 3, Willis does not recite a circuit that determines whether an address of write data, which is read from a recording medium, and an address of read data, which is provided to an encoder from a buffer memory, is the same. That is, Willis does not recite a circuit for determining whether addresses of data are the same. Accordingly, Willis does not disclose the first entry determination circuit of the present invention.

(3) Second entry determination circuit

Regarding the entry determination circuit, the Examiner applies the same reason as that of the first entry determination circuit. The second entry determination circuit of the present invention determines whether a timing for reading write data from a recording medium and a timing for encoding read data read from a buffer memory are the same. When data synchronization is taken by the synchronizing circuit, these timings are the same.

In contrast, although Willis describes a bit rate at Figs. 1 and 3, Willis does not recite a circuit that determines whether a timing for reading write data from a recording medium and a timing for encoding read data read from a buffer memory are the same. Accordingly, Willis does not disclose the second entry determination circuit of the present invention.

(4) Restart circuit

Because Willis does not describe the first and second entry determination circuit of the invention recited in claim 1, Willis can not disclose a restart circuit that restarts the writing of data to a recording medium based on the determinations of the first and second retry determination circuits.

Arataki also does not disclose the first retry determination circuit and the second retry determination circuit of the present invention. That is, Arataki does not disclose a circuit whether addresses or timings are the same. Rather, Arataki discloses a technique for improving the operation stability of a disk recording system with jitter free.

Independent Claim 3

Claims 3-5 and 7-9 were rejected as being unpatentable over Willis in view of Arataki. Applicant traverses this rejection.

Willis does not disclose a data recorder for writing to a recording medium including, among other features, 1) a synchronizing circuit for synchronizing the written data read from the recording medium with the encoded data, 2) a first retry determination circuit for determining whether an address of written data, which is read from a recording medium, and a write data address, which is stored in one or more address memories, are the same, and for determining whether an address of read data, which is provided to an encoder from a buffer memory, and a read data address, which is stored in the one or more address memories, are the same, 3) a second retry determination circuit for determining whether a timing for reading the written data from the recording medium and a timing for encoding the read data are the same, and 4) a restart circuit for restarting the writing of data to the recording medium based on the determinations of the first and second retry determination circuits. That is, Willis does not disclose a circuit that determines whether addresses are the same and timings are the same. Rather, Willis discloses data buffer management and a method for assigning record segments and play back recorded segments on a disk after a pause.

Arataki does not disclose the first retry determination circuit and the second retry determination circuit of the present invention of claim 3. As discussed above, Arataki does not disclose a circuit whether addresses are the same and timings are the same.

We further submit that because claims 4-6 depend from independent claim 3, these dependent claims are patentable for at least the same reasons that claim 3 is patentable.

Independent Claim 7

Willis does not disclose a data recorder for writing to a recording medium including, among other features, 1) a synchronizing circuit for synchronizing the written data read from the recording medium with the encoded data, 2) a retry determination circuit for determining whether an address of written data, which is read from a recording medium, and a write data address, which is stored in one or more address memories, are the same, and for determining whether an address of read data, which is provided to an encoder from a buffer memory, and a read data address, which is stored in the one or more address memories, are the same, 3) a synchronizing circuit that determines whether a timing for reading the written data from the recording medium and a timing for encoding the read data are the same, and 4) a restart circuit for restarting the writing of data to the recording medium based on the determinations of the retry determination circuit and the synchronizing circuit. That is, Willis does not disclose a circuit that determines whether addresses or timings are the same. Rather, Willis discloses data buffer management and a method for assigning record segments and play back recorded segments on a disk after a pause.

Arataki does not disclose the first retry determination circuit and the second retry determination circuit of the present invention of claim 7. As was the case with independent claims 1 and 3, neither Willis nor Arataki disclose a circuit whether addresses are the same and timings are the same.

We further submit that because claims 8-10 depend from independent claim 7, these dependent claims are patentable for at least the same reasons that claim 7 is patentable.

Enclosed is a check for the Petition for Extension of Time fee ($110 -- one month). Please apply any other charges, not covered, or credits to deposit account 06-1050, referencing Attorney Docket Number 10449-033001.

Respectfully submitted,

Date: September 18, 2005

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